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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,051	02/17/2004	Edward Flaherty	ALT-195 CON (A612 C1)	8388

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EXAMINER	
LEVIN, NAUM B	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 04/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/781,051	FLAHERTY ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/781,051 filed on 02/17/2004. Claims 1-40 remain pending in the application.

Claim Objections

2. Claims 1, 6, 8, 9, 17, 26, and 35 are objected to because following informalities:

3. Claim 1:

line 8, replace "data" with – a data --;

line 11, replace "data" with – said data --.

4. Claim 6:

line 6, replace "data" with – a data/first data --;

line 7, replace "data" with – said data/said first data --;

line 12, replace "data" with – a data --;

line 14, replace "data" with – said second data –;

line 17, replace "data" with – said second data –.

5. Claims 8, 9, 17, 26 and 35 must be clarified the same way as claims 1 and 6.

6. Claim 9:

line 7, replace "chip" with – integrated circuit chip --.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-40 are rejected under 35 U.S.C. 102(e) as being unpatentable by Narasimhan et al. (US Patent 6,446,192).

7. As to claims 1, 6, 8, 9, 17, 26, and 35 Narasimhan discloses:

A method of configuring an integrated circuit chip that includes programmable logic circuitry, said method comprising (Abstract):

programming said programmable logic circuitry to function as communications port circuitry (A single self-contained and autonomous module for directly interfacing device control circuitry of a device to a client machine via a computer network, wherein ... device interface comprises ... a programmable input/output port- claims 1-5; A programmable I/O (PIO) interface 82 provides a set of lines for connecting to sensors, switches, indicators, actuators. In order to reduce the chip pin count, a device interface multiplexer 84 selectively connects one of the interface options to the external pins of the chip - col.16, ll.11-15, Fig.12) (col.4, ll.65-67; col.9, ll.21-39; col.15, ll.62-64; col.16, ll.5-15; claims 1-5);

establishing with said programmed programmable logic circuitry a connection between the said integrated circuit chip and an off-chip source of data for use in reprogramming said programmable logic circuitry (Standard TCP/IP provides the transport and network layers for passing data between the equipment 34 and the remote client 30. TCP/IP is the standard Internet protocol and provides a reliable

transport which handles all the necessary handshaking, error-checking, and re-try algorithms to guarantee data delivery and integrity- col.6, ll.35-41; Ethernet and serial PPP protocols are supported at the datalink layer of the device interface chip 36, giving the designer a choice of many physical network media including 10/100Base-T, Modem, Serial, and RF. An enhanced Web Server (HTTP) and E-mail Client (SMTP) are built into the chip 36, allowing a variety of client interfaces to be offered –col.6, ll.47-52) (col.4, ll.37-54; col.6, ll.30-58);

transferring data from said off-chip source to said integrated circuit chip using said connection (Standard TCP/IP provides the transport and network layers for passing data between the equipment 34 and the remote client 30-col.6, ll.35-36) (col.6, ll.30-46; col.12, ll.40-67; col.13, ll.1-3); and

using transferred data to reprogram said programmable logic circuitry to function as other than communications port circuitry (single network interface chip provides all the networking hardware, networking software and device interface elements necessary for network connectivity and web-based or network-based management of any device. It also enables monitoring and controlling of any device - col.2, ll.46-51; As is evident from the description above, the chip 36 is entirely generic and capable of being customized to interface with any device using any of the various device interfaces described above, and with any client via any of the various network interfaces – col.16, ll.23-27; For example, the configuration memory 86 ... might store an application specific applet customized for the device. The applet for the digital camera might contain a virtual interface to the camera and its internal features, while the applet for the industrial

machine might contain a virtual interface to its status and control circuitry- col.16, ll. 34-40) (col.2, ll. 40-67; col.16, ll. 23-40);

(6) A method of configuring an integrated circuit chip that includes programmable logic circuitry, said method comprising:

establishing with receiver/transmitter circuitry (A standard universal asynchronous receiver/transmitter (UART) block 64 provides an alternate network connection for using a serial line or modem –col.15, ll.49-52) a connection between said integrated circuit chip and an off-chip source of data (Standard TCP/IP provides the transport and network layers for passing data between the equipment 34 and the remote client 30. TCP/IP is the standard Internet protocol and provides a reliable transport which handles all the necessary handshaking, error-checking, and re-try algorithms to guarantee data delivery and integrity- col.6, ll.35-41) (col.4, ll.37-54; col.6, ll.30-58; col.15, ll.49-52);

transferring data from said off-chip source to said integrated circuit chip using said connection (col.6, ll.30-46; col.12, ll.40-67; col.13, ll.1-3);

programming Ethernet media access controller (MAC) circuitry with said transferred data (In the network interface, a physical interface 60 (receives transferred data from the client 30 over the network 32, Fig. 1B) converts between the analog signals on the physical networking medium (RF, wire, optical, etc.) and the digital signals processed by the other blocks of the chip. A media access control (MAC) block 62 appropriately controls access to the physical network. Each type of network (RF,

Ethernet, optical, etc.) requires a unique MAC functionality for that network type. Ethernet is the most common media in current use- col.15, ll.40-48);

establishing with said Ethernet MAC circuitry a second connection between said integrated circuit chip and a second off-chip source of data (Standard TCP/IP provides the transport and network layers for passing data between the equipment 34 and the remote client 30. TCP/IP is the standard Internet protocol and provides a reliable transport which handles all the necessary handshaking, error-checking, and re-try algorithms –col.6, ll.38-40; the Parallel Bus Interface between the chip and the device. ... In the pass through mode, illustrated in FIG. 8, the network interface chip 36 simply acts as a bidirectional data port. ... Bytes sent by the remote client 30 are presented to the device control circuitry 38 through the receive register. Handshake signals are used for data flow control. This mode is most useful for products that already implement a communication protocol over a parallel bus –col.13, ll.56-67) (col.6, ll.30-41; col.13, ll.56-67; col.14, ll.1-2);

transferring data from said second off-chip source to said integrated circuit chip using said second connection (col.6, ll.30-46; col.12, ll.40-67; col.13, ll.1-3); and

using transferred data from said second off-chip source to program said programmable logic circuitry (col.2, ll. 40-67; col.16, ll. 23-40);

(8) A method of configuring an integrated circuit chip that includes programmable logic circuitry, said method comprising:

establishing with receiver/transmitter circuitry a connection between said chip and an off-chip source of data (col.4, ll.37-54; col.6, ll.30-58; col.15, ll.49-52);

transferring data from said off-chip source to said chip using said connection (col.6, ll.30-46; col.12, ll.40-67; col.13, ll.1-3);

programming said programmable logic circuitry with said transferred data to function as Ethernet media access controller (MAC) circuitry (col.15, ll.40-48);

establishing with said programmed programmable logic circuitry a second connection between said integrated circuit chip and a second off-chip source of data (col.6, ll.30-41; col.13, ll.56-67; col.14, ll.1-2);

transferring data from said second off-chip source to said integrated circuit chip using said second connection (col.6, ll.30-46; col.12, ll.40-67; col.13, ll.1-3); and

using transferred data to reprogram said programmable logic circuitry to function as something other than said Ethernet MAC circuitry (col.2, ll. 40-67; col.16, ll. 23-40);

(9) An integrated circuit chip comprising:

programmable logic circuitry (col.4, ll.65-67; col.9, ll.21-39; col.15, ll.62-64; col.16, ll.5-15; claims 1-5);

processor circuitry operative to program said programmable logic circuitry (col.15, ll.40-67; col.16, ll.1-5); and

Ethernet media access controller (MAC) circuitry operative to establish a connection between said chip and an off-chip source of data, said Ethernet MAC circuitry coupled to said processor circuitry (A media access control (MAC) block 62 appropriately controls access to the physical network. Each type of network (RF, Ethernet, optical, etc.) requires a unique MAC functionality for that network type.

Ethernet is the most common media in current use- col.15, ll.40-48) (col.3, ll.30-33; col.4, ll.65-67; col.5, ll.11-16; col.6, ll.53-55; col.15, ll.40-55);

(17) An integrated circuit chip comprising:

programmable logic circuitry operative to be selectively programmed as communications port circuitry (col.15, ll.64-67; col.16, ll.1-14);

processor circuitry operative to program said programmable logic circuitry (col.15, ll.40-67; col.16, ll.1-5);

memory circuitry (Fig. 12: positions 68, 70, 74, 86);

Ethernet media access controller (MAC) circuitry operative to establish a connection between said chip and an off-chip source of data (col.3, ll.30-33; col.4, ll.65-67; col.5, ll.11-16; col.6, ll.53-55; col.15, ll.40-55); and

interconnection bus circuitry coupled to said programmable logic circuitry, processor circuitry, memory circuitry, and Ethernet MAC circuitry (col.15, ll.36-67; col.16, ll.1-22, Fig. 12, Abstract);

(26) An integrated circuit chip comprising:

programmable logic circuitry operative to be selectively programmed as communications port circuitry (col.15, ll.64-67; col.16, ll.1-14);

processor circuitry operative to program said programmable logic circuitry (col.15, ll.40-67; col.16, ll.1-5);

receiver/transmitter circuitry (col.15, ll.49-52);

Ethernet media access controller (MAC) circuitry operative to establish a connection between said chip and an off-chip source of data (col.3, ll.30-33; col.4, ll.65-67; col.5, ll.11-16; col.6, ll.53-55; col.15, ll.40-55); and

interconnection bus circuitry coupled to said programmable logic circuitry, processor circuitry, receiver/transmitter circuitry, and Ethernet MAC circuitry (col.15, ll.36-67; col.16, ll.1-22, Fig. 12, Abstract);

(35) An integrated circuit chip comprising:

programmable logic circuitry operative to be selectively programmed as Ethernet media access controller (MAC) circuitry (col.15, ll.43-67; col.16, ll.1-14);

processing circuitry operative to program said programmable logic circuitry (col.15, ll.40-67; col.16, ll.1-5);

receiver/transmitter circuitry (col.15, ll.49-52); and

interconnection bus circuitry coupled to said programmable logic circuitry, processing circuitry, and receiver/transmitter circuitry (col.15, ll.36-67; col.16, ll.1-22, Fig. 12, Abstract).

8. As to claims 2-5, 7, , 10-16, 18-25, 27-34, and 36-40 Narasimhan recites:

(2), (28) The method/IC, wherein said transferring data to a memory on said integrated circuit chip uses said connection (col.15, ll.36-67; col.16, ll.1-22, Fig. 12, Abstract);

(3), (13), (14), (22), (23), (31), (32) The method/IC, wherein said programming comprises programming to function as Ethernet media access controller (MAC) circuitry (col.3, ll.30-33; col.4, ll.65-67; col.5, ll.11-16; col.6, ll.53-55; col.15, ll.40-55);

(4), (5) The method further comprising before said programming establishing a first connection between said integrated circuit chip and a first off-chip source of data (col.4, ll.37-54; col.6, ll.30-58; col.12, ll.40-67; col.13, ll.1-3col.15, ll.49-52);

(7) The method, wherein programming Ethernet MAC circuitry uses a speed of operation (col.15, ll.1-35);

(10), (19) The integrated circuit chip, wherein said processor circuitry is microprocessor circuitry (col.5, ll.20-23);

(11), (27) The integrated circuit chip, wherein said programmable logic circuitry is reprogrammable (col.2, ll. 40-67; col.16, ll. 23-40);

(12), (21), (30), (36), (37), (38) An end-user system comprising a circuit board comprising: a processor; a memory; 1/0 circuitry (Abstract; Fig.3- client hardware);

(15), (16), (18), (24), (25), (33), (39), (40) The end-user system, wherein said end-user system comprises a data processing system (Abstract);

(20), (29) The integrated circuit, wherein said memory circuitry is random access memory (RAM) (col.15, ll.62-64).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NL

THUAN DO
Primary examiner -
04/13/2006